



***3 Volt Intel[®] StrataFlash[™]
Memory to Intel[®] StrongARM^{*}
SA-1110 CPU Design Guide***

Application Note 698

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Revision History

Date of Revision	Version	Description
07/20/99	-001	Original version
04/06/00	-002	Reformatted document

1.0 Introduction

3 Volt Intel® StrataFlash™ memory provides reliable two-bit-per-cell technology at a low cost. This product offers higher performance than previous 5 Volt Intel® StrataFlash™ memory with faster read times and a page-mode interface for increased speed. Other benefits include more density in less space, high-speed interface, support for code and data storage in the same device, and Common Flash Interface (CFI) for easy migration to future devices.

This application note will cover the 3 Volt Intel StrataFlash memory interfaces to Intel® StrongARM* microprocessor.

This document was written with preliminary information about 3 Volt Intel StrataFlash memory. Any changes in those specifications may not be reflected in this document. These interfaces have not been implemented in hardware. Refer to the appropriate documents or sales personnel for the most current information.

2.0 Hardware Interface

This section describes signals and considerations that occur in most of the interfaces.

The interfaces in this document use the following signals generated by the 3 Volt Intel StrataFlash memory:

V_{CC} : Device power supply. 2.7 V – 3.6 V

V_{CCQ} : Output buffer power supply. This voltage controls the device's output voltages. 5 V \pm 10% or 2.7 V – 3.6 V

OE#: Output enable is an active low signal that activates the device's outputs during a read operation. Any data remaining on the bus after this signal is driven high will be lost. This signal must remain inactive during a write operation.

WE#: Write enable is an active low signal that controls writes to the Command User Interface, write buffer, and array blocks. The rising edge of this signal latches addresses and data. WE# must remain inactive during read access, and must toggle between consecutive writes.

CE_{0,2}: The three chip enable signals activate the device's control logic, input buffers, decoders, and sense amplifiers. Multiple chip enable signals allow switching between several 3 Volt Intel StrataFlash memory components without additional decoding. For all designs in this document, CE₁ and CE₂ are tied to ground. CE₀ is used as the only signal to enable the device. Chip enable signals must remain in an active state during any read or write access. When the CE pins disable the 3 Volt Intel StrataFlash memory, the device is deselected and power consumption is reduced to standby levels. For more information on typical CE configurations see the *3 Volt Intel® StrataFlash™ Memory: 28F128J3A, 28F640J3A, 28F320J3A* datasheet.

RP#: Reset/Power Down is an active low signal. It resets internal automation and puts the device in power-down mode. Exit from reset sets the device in read array mode with page-mode disabled. After exiting from reset or powering on the 3 Volt Intel StrataFlash memory, bit 16 of the read control register must be set to enable page-mode timings.

BYTE#: Byte enable is an active low signal. Byte enable low places the 3 Volt Intel StrataFlash memory in x8 mode. Byte enable high places the 3 Volt Intel StrataFlash memory in x16 mode.

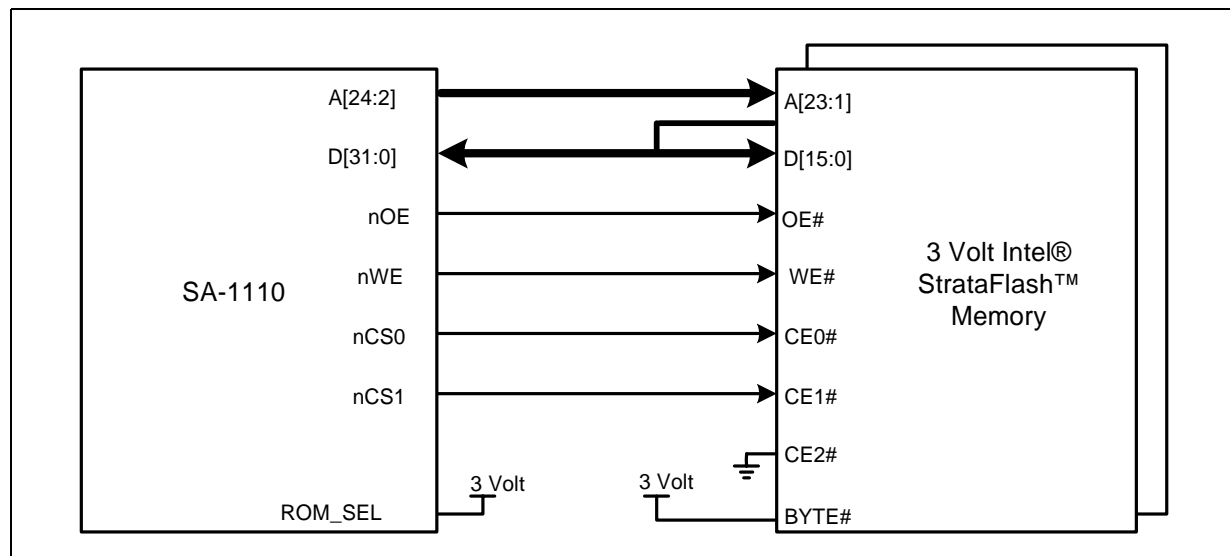
This document assumes all other pins (e.g., Address, Data, etc.) are connected in such a way as to insure proper device functioning.

3.0 Interfacing the 3 Volt Intel® StrataFlash™ Memory to Intel® StrongARM* SA-1110 at 66 MHz

By setting certain registers, this reference design is a glueless interface between the 3 Volt Intel StrataFlash and the Intel StrongARM SA-1110. The designers should use two 128-Mbit Intel StrataFlash memory devices to match the 32-bit data bus of the SA-1110.

Figure 1 illustrates the block diagram of the 3 Volt Intel StrataFlash memory interfaces to the StrongARM SA-1110.

Figure 1. The 3 Volt Intel® StrataFlash™ Memory Interfaces to the Intel® StrongARM* SA-1110 Microprocessor



3.1 Interface Considerations

By setting certain registers, this reference design is a glueless interface between 3 Volt Intel StrataFlash memory and the StrongARM SA-1110. The designers should use two 128-Mbit Intel StrataFlash memory to match the 32-bit data bus of the SA-1110.

This sample interface uses two 3 Volt Intel StrataFlash memory devices in 16-bit mode. Timing diagrams were made with the 128-Mbit 3 Volt Intel StrataFlash components with the memory bus running at 66 MHz. There is no other required logic between the processor and the 3 Volt Intel StrataFlash memory.

This reference interface in this document uses page-mode timings. Before the 3 Volt Intel StrataFlash memory's page-mode timings can be used, Read Configuration Register bit 16 (RCR.16) must be set to b'1 to enable the page-mode.

3.2 Processor Interface Signals

This interface uses the following signals provided by the SA-1110:

A₂₅–A₀: The 25-bit address bus transmits instruction and data addresses to memory.

D₃₁–D₀: The bi-directional data bus transfers data between the processor and memory.

NCS(3:0): These signals are chip selects to static memory devices.

OE: Output Enable indicates the memory output enable.

WE: Write Enable indicates to memory that writes are enabled.

ROM_SEL: ROM Select. This pin is used to configure the ROM width. If it is grounded, the ROM width is 16 bits. If it is pulled high, the ROM width is 32 bits.

3.3 Control Signal Generation

Figure 2 shows a four-word page-mode read timing diagram. For this four flash read, the RDF[7:3] should be set h'0A, RDN[12:8] should be set to h'02 and RRR[15:13] should be set h'1 in the MSC0 register.

Figure 2. The 3 Volt Intel® StrataFlash™ Memory/Intel® StrongARM® SA-1110 Four-Word Page-Mode Read Cycle at 66 MHz

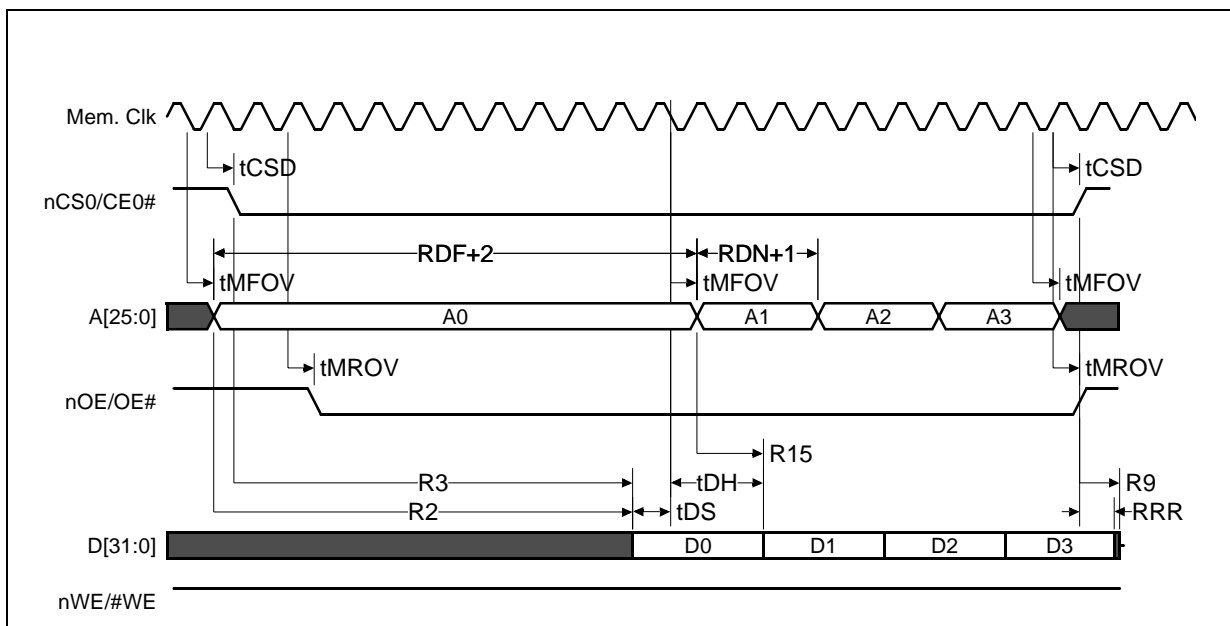


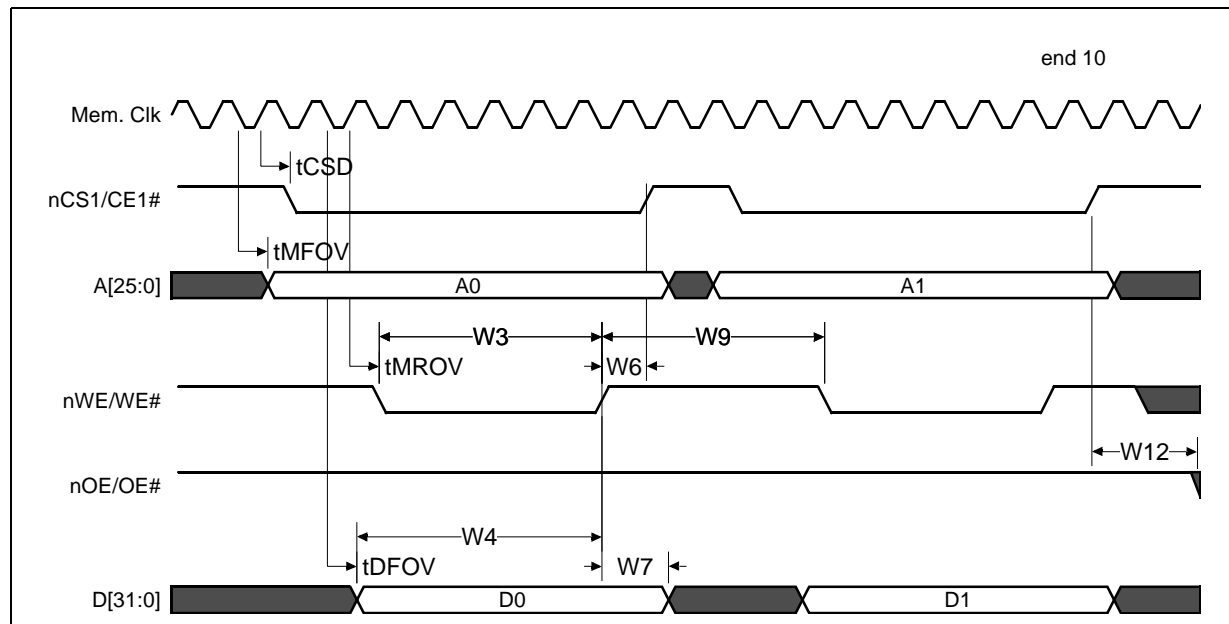
Figure 3 shows the write timing diagram. RDN[12:8] should be set to b'0100 in the MSC1 register.

The following signal can be found in the *Intel® StrongARM® SA-1110 Microprocessor Advanced Developer's Manual* manual: t_{CSD} , t_{MFOV} , t_{MROV} , t_{DS} , t_{DH} , RDF, RDN, RRR.

The following signal can be located in the *3 Volt Intel® StrataFlash™ Memory: 28F128J3A, 28F640J3A, 28F320J3A* datasheet: R2, R3, R9, R15.

Read all appropriate documentation before attempting this interface.

Figure 3. The 3 Volt Intel® StrataFlash™ Memory/Intel® StrongARM® SA-1110 Write Timing Diagram at 66 MHz



4.0 Summary

The 3 Volt Intel StrataFlash memory devices provide 2X the bits in 1X the space. These devices provide reliable two-bit-per-cell storage technology. Faster performance can be enabled by setting RCR bit 16 to enable page-mode reads. The 3 Volt Intel StrataFlash memory devices are able to have different I/O voltages by using different V_{CCQ} voltages. The 3 Volt Intel StrataFlash memory components come in a variety of different packages and densities for increased flexibility. This “glueless” interface reduce power consumption. It is an excellent option for code and data applications where high density and low cost are required.

Appendix A Additional Information

Order Number	Document/Tool
290667	<i>Intel® StrataFlash™ Memory; 28F128J3A, 28F640J3A, 38F320J3A datasheet</i>
298130	<i>Intel® StrataFlash™ Memory; 28F128J3A, 28F640J3A, 38F320J3A Specification Update</i>
297859	<i>AP-677 Intel® StrataFlash™ Memory Technology</i>
292222	<i>AP-664 Designing Intel® StrataFlash™ Memory into Intel® Architecture</i>
292221	<i>AP-663 Using the Intel® StrataFlash™ Memory Write Buffer</i>
292218	<i>AP-660 Migration Guide to 3 Volt Intel® StrataFlash™ Memory</i>
292204	<i>AP-646 Common Flash Interface (CFI) and Command Sets</i>
292172	<i>AP-617 Additional Flash Data Protection Using V_{PP} RP#, and WP#</i>
278240	<i>Intel® StrongARM® SA-1110 Microprocessor Advanced Developer's Manual</i>

NOTES:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at <http://www.intel.com> for technical documentation and tools.
3. For the most current information on Intel StrataFlash memory, visit our website at <http://developer.intel.com/design/flash/isf>.

